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Source-All-Around Tunnel Field-Effect Transistor (SAA-TFET): Proposal and Design

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Abstract

In this paper, a new source-all-around tunnel field-effect transistor (SAA-TFET) is proposed and investigated by using TCAD simulation. The tunneling junction in the SAA-TFET is divided laterally and vertically with respect to the channel direction which provides a relatively large tunneling junction area. An n+ pocket design is also introduced around the source to enhance tunneling rates and improve the device characteristics. In addition, the gate and n+ pocket region also overlap in the vertical and the lateral directions resulting in an enhanced electric field and, in turn, the ON-state current of the SAA-TFET is highly increased compared with the conventional TFET. Promising results in terms of DC (I_{ON}, I_{OFF}, ON/OFF current ratio and *SS*) and analog (cutoff frequency) performance are obtained for low (V_{DD} = 0.5 V) and high (V_{DD} = 1 V) supply voltages.

Keywords

Band-to-Band Tunneling (BTBT); Source-all-around; tunnel field-effect transistor (TFET); n+ pocket

Introduction

In order to overcome the problems arising from scaling limitation of conventional MOSFETs, extensive research work has been directed to develop novel device structures. Multi-gate FETs and nanowire MOSFETs are examples of such research progress. Although the mentioned devices show enhancements in device performance, reducing power dissipation in electronic circuits is becoming a challenge that prevents further advances regarding these structures [1]. One of the most arising novel devices to improve the energy efficiency is the Tunneling FET (TFET) which is considered an attractive candidate to replace MOSFET for low power applications as it possesses extremely low leakage current (I_{OFF}), sub-60-mV/dec subthreshold swing (*SS*) and low standby power consumption. Both experimental and simulation work have been provided and demonstrated that TFETs could replace or work along MOSFETs in a hybrid circuitry to provide power saving [1].

However, experimental TFETs commonly suffer from low ON-current (I_{ON}) and ambipolar conduction (I_{AMB}). To overcome these issues, several TFET structure modifications have been proposed. For controlling the channel through gate voltage and boosting I_{ON} in TFETs, the tunneling barrier height and/or tunneling width should be reduced. In this regard, many device and material engineering techniques have been proposed such as dual material gate [2], hetero-gate dielectric [3], thin high-

doped pocket between the source and channel [4, 5], small band gap materials [6, 7, 8]. Other techniques are also found in literature [9, 10, 11].

One of the most promising techniques is multi-gate architecture TFETs (double gate, gate all around architectures) [12]. Gate-All-Around (GAA) nanowire TFETs [13] have been in spotlight because of their excellent gate controllability and recent progress in top-down planar process [14, 15]. Because of their good electrostatic gate-control, they can suppress the OFF-state leakage current and short-channel effect (SCE) and provide a high ON-state current at low supply voltage. In addition, the area occupied by vertical FETs is smaller than that occupied by planar FETs which leads to high device density [16, 17]. Moreover, a vertical integration of TFETs [18] benefits from a lesser complex implementation of a heterojunction at the source in order to boost the tunneling efficiency [19]. Vertical nanowires with a cylindrical shape can be grown with a metal nanoparticle as a catalyst [20] or etched (and oxidized) by using a patterned mask [18, 21]. The vertical SiNW (Silicon Nanowire) platform is ideal for TFET fabrication, as source and drain implants can be independently controlled without lithography [18].

There are two mechanisms of BTBT in TFETs: line (or vertical) and point (or lateral) tunneling. The latter involves a source-channel lateral tunneling along the transport direction and its dominant contribution is localized in a small area; while, regarding line tunneling, there is a vertical tunneling component which is perpendicular to the channel direction resulting from the alignment of the tunneling path with the electric field of the gate. It is argued that line tunneling gives much higher I_{ON} and better *SS* than point tunneling [22].

The tunneling area of the source–channel junction has increased by using structural engineering in such a way that the more carriers are tunneled in the channel region as introduced by L-shaped [23] and U-shaped TFET [21]. Kim *et al.* [24], [25]

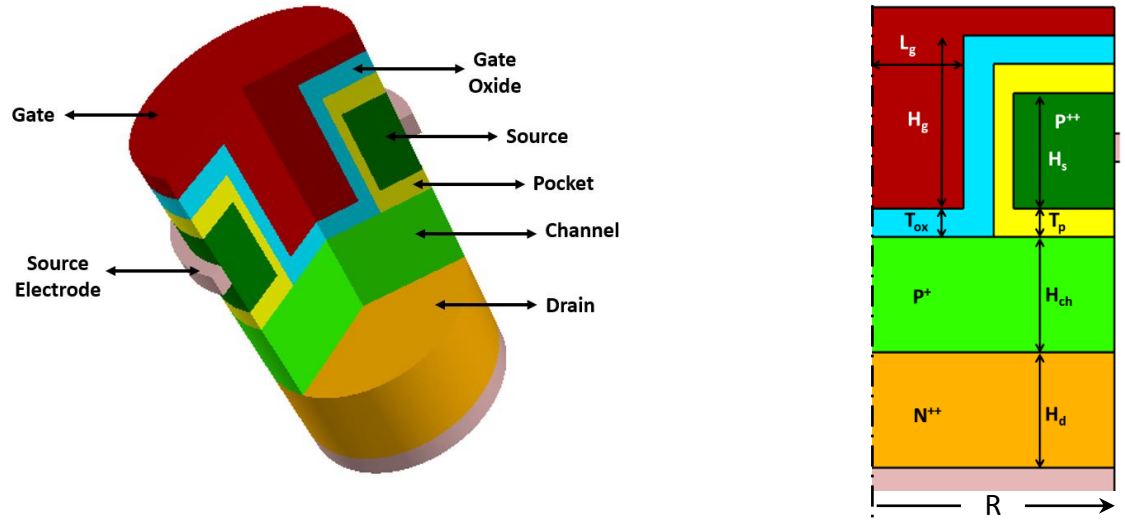
proposed and experimentally demonstrated the L-shaped TFET for higher I_{ON} and smaller *SS* but at the cost of higher turn-ON voltages. In addition, the tunnel junction cross-sectional area can be increased depending on the gate and source overlaps, in contrast to conventional TFETs [26, 27]. Moreover, to improve the performance characteristics of the vertical TFET, several methods have been proposed. Counter doping at the interface between the source and gate dielectric [26] and dual or gradual gates with different work functions [28] while improving performance, also make process and circuit design of vertical BTBT-based TFETs more challenging [29].

In this work, we propose a new design of TFETs, based on line tunneling, in which the source electrode is all around the structure. The performance parameters are measured as follows: *SS,* I_{ON}*,* I_{OFF} and ON to OFF current ratio are inspected as main DC parameters; while, the transconductance (g_m) and unity-gain cutoff frequency (f_T) are analyzed as main high-frequency parameters. These analog figures of merit are extracted from the small signal ac analysis at 1 MHz [30]. The design of the proposed TFET is performed by using TCAD simulation.

Device Structure and Simulation Models

Fig. 1 shows a 3D (Fig. 1(a)) and cross-sectional view (Fig. 1(b)) of the proposed cylindrical n-channel SAA-TFET. The device under investigation has the following technological and geometrical parameters: p-type channel region doping = 10^{17} cm^{-3}, p-type source doping = 10^{20} cm^{-3} and n-type drain doping = 10^{19} cm^{-3}. All regions are assumed uniform in their doping profiles and the source-channel junction is kept abrupt. A pocket is designed to be all around the source and having an n-type doping of 10^{19} cm^{-3}. The oxide thickness (t_{ox}) is 3 nm utilizing HfO_2 as the gate insulator with

a relative permittivity of ε_{ox} = 21 and the gate work function is taken to be φ = 4.17 eV. The other parameters (like channel radius (R), height of the source region H_s, height of the drain region H_d, height of the gate H_g, width of the gate region L_g and pocket thickness t_p) are considered as design parameters and their values may change throughout this study.



(a) (b)

Fig. 1: Schematic description of the proposed SAA NW TFET: (a) 3-D simulated structure and (b) cross-sectional view of the device.

Device simulations are carried out by using Silvaco TCAD [31]. In our analysis, the nonlocal band-to-band tunneling (BTBT) model, implemented in Silvaco/Atlas device simulator, is employed [32]. In this perspective, the tunnel current is generated near the source/pocket/channel and channel/drain junction. The mesh has been refined carefully in the tunneling zones (both source/pocket and channel/drain interfaces). Due to the presence of high doping concentration in the pocket, source and drain regions, band gap narrowing (BGN) model is also included along with Fermi-Dirac statistics (FERMI) instead of Boltzmann statistics [33]. Lombardi model (CVT) is activated to express carrier mobility which combines transverse and parallel electric

field, doping and temperature effects. Furthermore, models for carrier recombination Shockley–Read–Hall (SRH) and Auger are also adopted. Mid-gap traps are accounted for by SRH generation-recombination processes [34]. Moreover, trap-assisted tunneling (TAT) is enabled using the default values of the simulator [31, 35]. Additionally, gate leakage current is neglected as long as $V_{GS} \leq V_{DS}$ [36]. Finally, quantum confinement effects are ignored.

To calibrate the nonlocal BTBT model, the electron mass (m_e) and hole mass (m_h) for silicon are set to 0.11 and 0.17, respectively [37]. For a validity check regarding these values, a comparison between an experimental GAA Si-TFET structure and our simulation is performed. The results of the transfer characteristics (I_D-V_{GS}) are shown in Fig. 2 given V_{DS} = 1 V. It can be inferred from the comparison that there is a good agreement between measurements and simulation based on the selected models and physical parameters. As shown, the IV curve is divided into different regions. Regarding the OFF state, SRH and TAT models are of great impact. Enabling TAT and default values of SRH lifetimes in simulation gives one order of magnitude lower OFF current than measurements; while, by adjusting the values of the lifetimes (τ_{n0} = τ_{n0} = 5 ns), the simulated OFF current is fitted well with experimental values. Further, to adjust current values for higher V_{GS} values, an interface charge is added (of value 1×10^{12} cm^{-3}). The interface charge is located at the surface between the gate oxide and the channel region. For high gate voltages, BTBT current is dominated.

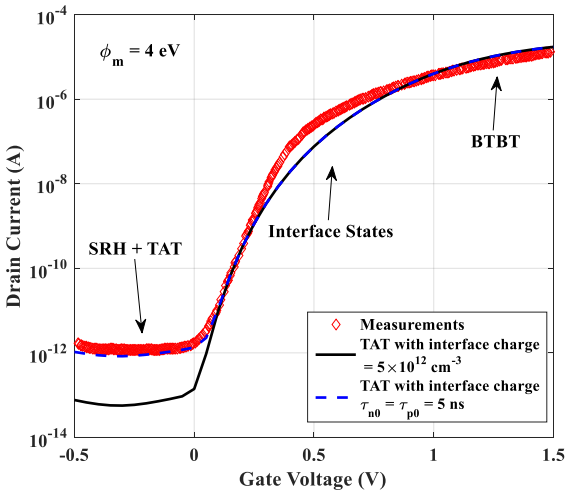


Fig. 2: Transfer characteristics calibration against the results reported in [18], taking the gate work function ϕ_m = 4 eV.

Results and Discussion

In the following simulations, two cases for the terminal voltages are considered to study both low- and high-power supply, the first is when V_{DS} = 0.5 V for the range 0 ≤ V_{GS} ≤ 0.5 V and the other is when V_{DS} = 1 V for the range 0 ≤ V_{GS} ≤ 1 V. In order to examine the device performance, concerning both DC and analog behavior, some key factors are defined. The ON current (I_{ON}) is defined as the drain current at the maximum gate voltage (V_{GSmax}) (i.e. V_{GS} = 1 V in the case of V_{DS} = 1 V, while V_{GS} = 0.5 V in the case of V_{DS} = 0.5 V). The OFF current (I_{OFF}) is defined as the drain current at which V_{GS} = V_{OFF} where V_{OFF} is the voltage at which the current begins directly to increase leaving the OFF state. The threshold voltage (V_t) is the gate voltage at which the drain current is 10^{-7} A/μm [32] while the subthreshold swing is defined as the average *SS*, which is the inverse slope extracted from the transfer characteristics from the point at which I_{OFF} is extracted to the point at which the drain current I_D = 10^{-7} A/μm and it is defined as follows [1, 32],

$$SS_{av} = -\frac{V_t - V_{OFF}}{\log\left(10^{-7}\right) - \log\left(I_{OFF}\right)} \qquad (1)$$

Regarding the analog behavior, the cutoff frequency is selected as a figure of merit (FOM) where it can be extracted using advanced two port network by the unit-gain-point method which gives [38],

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{\left(1+2C_{gd}/C_{gs}\right)}} \approx \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)} \qquad (2)$$

where g_m is the transconductance and $C_{gs} + C_{gd} = C_{gg}$ is the total gate-to-gate capacitance.

Now, the device parameters are initialized as follows. The wire radius (R) is 50 nm, the gate length (L_g) and the pocket thickness (t_p) are chosen to be 10 nm and 4 nm, respectively. The source height (H_s) is fixed at 30 nm while channel height (H_{ch}) is 10 nm. Fig. 3 shows the results of DC and analog device characteristics. Here, the DC performance is measured in terms of the transfer characteristics I_D-V_{GS} while the cutoff frequency is used as an analog FOM.

Fig. 3(a) shows both DC and analog performance at V_{DS} = 0.5 V (for the range 0 ≤ V_{GS} ≤ 0.5 V), while Fig. 3(b) shows the performance at V_{DS} = 1 V (for the range 0 ≤ V_{GS} ≤ 1 V). For V_{DS} = 1 V, the cutoff frequency increases up to a certain value of V_{GS} and then decreases. This is due to mainly the behavior of transconductance of the device. The transconductance depends chiefly on the rate of drain current. The greater increasing rate of drain current is, the higher transconductance. So, as V_{GS} increases, g_m increases, up to V_{GS} = 0.8 V as shown, due to the enhancement of current driving capability. However, for V_{GS} > 0.8 V, the cutoff frequency drops as g_m drops due to mobility degradations. The main performance measures for the initial device parameters are illustrated in Table 1 for both cases of V_{DS} = 0.5 V and V_{DS} = 1 V.

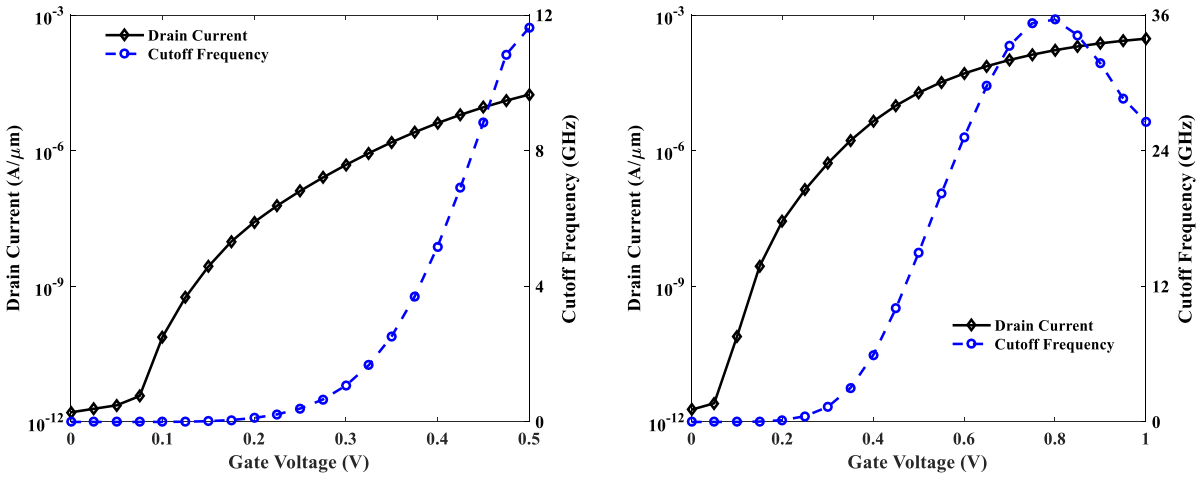


Fig. 3: Transfer characteristics and cutoff frequency for (a) V_{DS} = 0.5 V and (b) V_{DS} = 1 V.

Table 1 Main performance device parameters for initial device dimensions

	I_{ON} ×10^{-5} (A/μm)		I_{OFF} ×10^{-13} (A/μm)		I_{ON}/I_{OFF} ×10^{7}		V_t (V)		SS (mV/dec)		f_{Tmax} (GHz)	
V_{DS} (V)	0.5	1	0.5	1	0.5	1	0.5	1	0.5	1	0.5	1
Value	1.73	29.7	0.163	0.185	1.05	16.20	0.246	0.241	32.87	37.40	11.6	35.5

To gain more physical insight about the operation of the device, Fig. 4 shows the contour diagrams of the potential, electric field, BTB hole tunneling rate and hole concentration at V_{GS} = 1 V and V_{DS} = 1 V. It can be inferred from Fig. 4(a) that the potential bends significantly between the source and pocket which results in enhancing the tunneling efficiency in both the lateral and vertical directions. This bending is reflected on the electric field (Fig. 4(b)) and hole BTBT rate (Fig. 4(c)) unlike the case of L-shaped Gate TFET (LG-TFET) which produces BTBT rates mainly in the vertical direction [39]. Moreover, the contour plot of the concentration of induced holes in the source is illustrated in Fig. 4(d). It is observed that the induced

surface carrier concentration is significantly large around the whole area of the source which is required for the appropriate operation of a transistor [40].

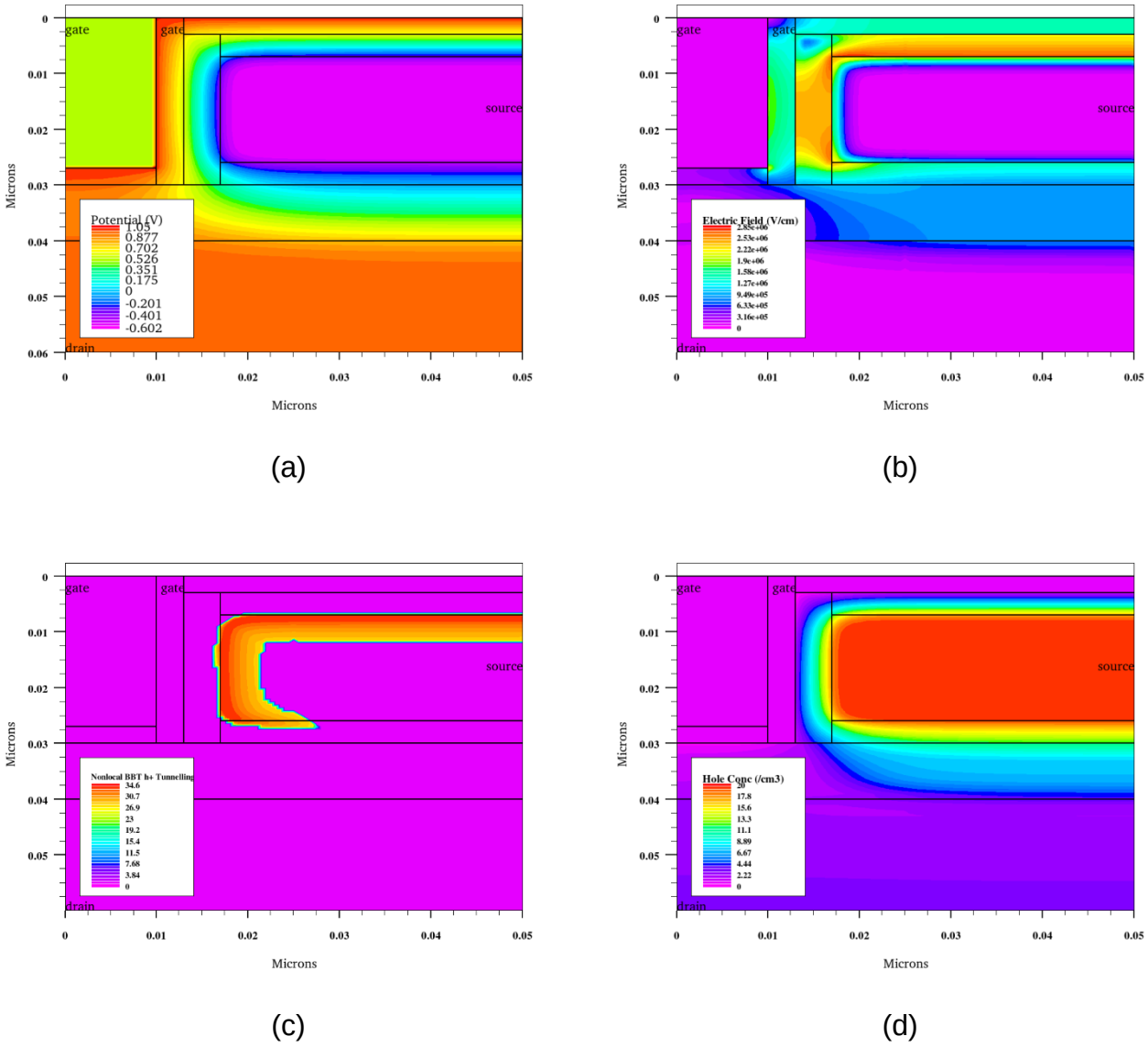


Fig. 4: Contour plots of (a) Potential, (b) electric field (c) Non-local BTB hole tunneling rate and (d) hole concentration.

Impact of design parameters variation

In this subsection, the impact of design parameters variation on device performance, in terms of both DC and analog behavior, is examined. Regarding the DC performance, I_{ON}, I_{OFF}, ON/OFF current ratio, V_t and *SS* are chosen as key

parameters for determining the performance. On the other hand, when regarding the analog performance, it is measured by the maximum cutoff frequency (f_{Tmax}) which is the maximum obtainable value for the whole range of the gate voltage.

Impact of H_s

In the following simulation, the device parameters are chosen as follows: R = 50 nm, L_g = 10 nm, t_p = 4 nm. Then, H_s is varied from 30, 40 and 50 nm and the results are reported in Table 2. It is evident that increasing H_s deteriorates all device performance parameters as it causes decreasing of I_{ON}, ON/OFF ratio and f_{Tmax} while it increases both V_t and SS. So, a choice of 30 nm is suitable for our design.

To gain a physical insight about the effect of H_s on the ON current, the energy band structure is drawn with two different H_s values (namely, 30 and 40 nm) as shown in Fig. 5. The inset in the figure shows the horizontal cut line location through which the energy band is drawn (which is 1 nm below the pocket). It can be observed from the energy band diagram that the lower value of H_s gives a larger tunneling window and less tunneling widths are also obtained which, in turn, results in higher BBT rates and, consequently, more I_{ON}.

Table 2 Impact of H_s on main performance device parameters

Parameter	I_{ON} ×10^{-5} (A/μm)		I_{OFF} ×10^{-13} (A/μm)		I_{ON}/I_{OFF} ×10^{7}		V_t (V)		SS (mV/dec)		f_{Tmax} (GHz)	
V_{DS} (V)	0.5	1	0.5	1	0.5	1	0.5	1	0.5	1	0.5	1
H_s = 30 nm	1.73	29.7	0.163	0.185	1.05	16.20	0.246	0.241	32.87	37.40	11.6	35.5
H_s = 40 nm	1.10	24.3	0.139	0.158	0.79	15.50	0.274	0.264	37.60	41.43	8.6	31.5
H_s = 50 nm	0.81	20.7	0.123	0.140	0.67	14.90	0.290	0.284	40.46	44.46	7.0	29.0

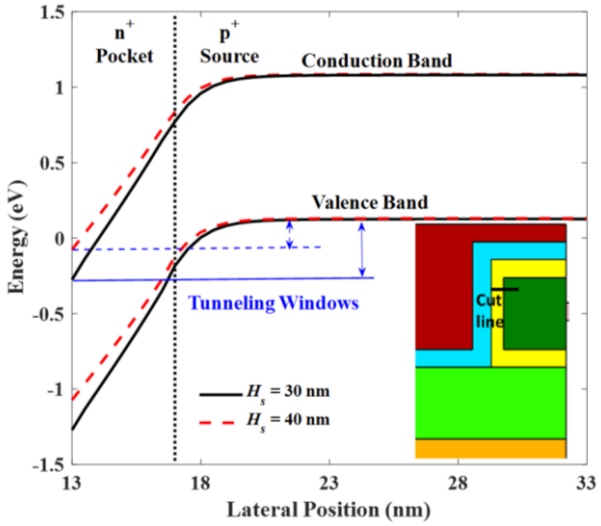


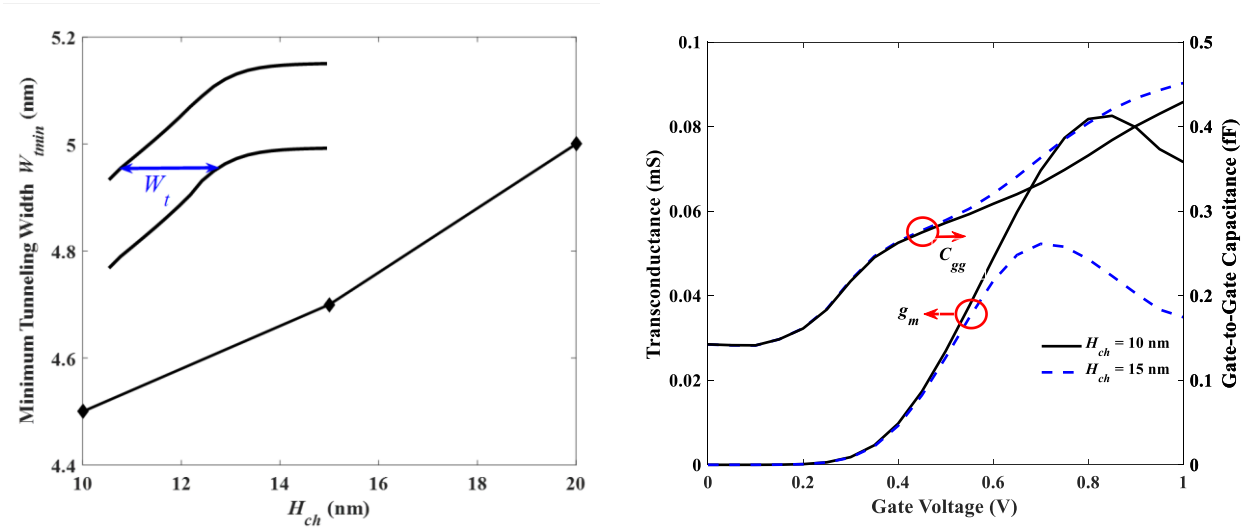
Fig. 5: Energy band diagrams from pocket to source region (5 nm below the oxide interface) (at V_{DS} = 1 V and V_{GS} = 1 V).

Impact of H_{ch}

Next the effect of H_{ch} is studied. Table 3 gives the main performance device parameters with the variation of H_{ch}. Increasing H_{ch} deteriorates both DC and analog performance. So, a choice of H_{ch} = 10 nm is suitable to proceed the design. Fig. 6 explains the effect of H_{ch} in terms of DC (Fig. 6a) and analog performance (Fig. 6b). Fig. 6a shows the minimum tunneling width for different values of H_{ch}. It can be inferred that increasing H_{ch} results in increasing the minimum tunneling width which causes lower I_{ON} values. In addition, Fig. 6b shows the influence of H_{ch} on the transconductance and total gate-to-gate capacitance. The figure illustrates that increasing H_{ch} causes slightly higher capacitance and lower transconductance which deteriorates the cutoff frequency as depicted from Table 3.

Table 3 Impact of H_{ch} on main performance device parameters

Parameter	I_{ON} ×10^{-5} (A/μm)		I_{OFF} ×10^{-13} (A/μm)		I_{ON}/I_{OFF} ×10^{7}		V_t (V)		SS (mV/dec)		f_{Tmax} (GHz)	
V_{DS} (V)	0.5	1	0.5	1	0.5	1	0.5	1	0.5	1	0.5	1
H_{ch}= 10 nm	1.73	29.7	0.163	0.185	1.05	16.2	0.246	0.241	32.87	37.40	11.6	35.5
H_{ch}= 15 nm	1.46	20.2	0.157	0.166	0.93	15.9	0.249	0.244	33.17	37.40	8.0	23.0
H_{ch}= 20 nm	0.95	12.7	0.155	0.159	0.61	8.3	0.252	0.247	33.60	37.57	4.0	14.0



(a) (b)

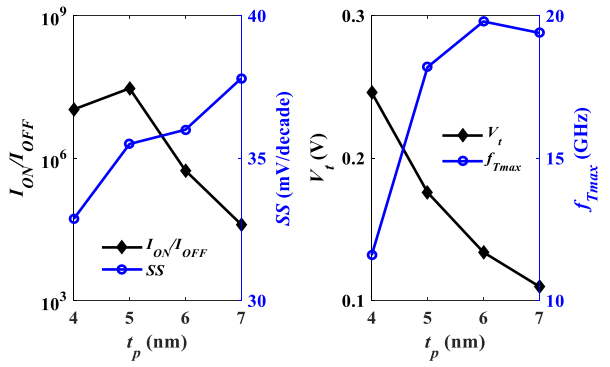
Fig. 6: Impact of H_{ch} (a) Minimum tunneling width in the ON state (V_{DS} = 1 V and V_{GS} = 1 V) and (b) Transconductance and gate-to-gate capacitance variation with V_{GS} at V_{DS} = 1 V.

Impact of t_p

Next, the impact of t_p is studied for V_{DS} = 0.5 V for the range 0 ≤ V_{GS} ≤ 0.5 V. Regarding the ON/OFF ratio, there is an optimum value which is t_p = 5 nm as shown in Fig. 7. When considering threshold voltage and SS, although their values at t_p = 5 nm are not the minimum, they are not much higher than the values occurring at thicker t_p. The criterion is similar for f_{Tmax} as it increases when t_p increases; however, the value of f_{Tmax} (18.2 GHz) at t_p = 5 nm is not far from the maximum value (19.8

GHz) which occurs at t_p = 6 nm. So, it is suitable to choose t_p = 5 nm to continue our design. The same behavior holds if V_{DS} is 1 V.

For a physical explanation of the OFF current rise when increasing t_p, Fig. 8 gives the energy band diagram at the OFF state (V_{DS} = 1 V and V_{GS} = 0 V) for t_p = 5 and 6 nm. The energy band diagrams are drawn through a vertical cut line as shown in the inset Fig. 8. It is observed that when increasing t_p, a tunneling window begins to appear which enhances the tunneling flow in the OFF state and hence increases the OFF current. On the other hand, when t_p = 5 nm, there is no tunneling window and tunneling rates are, consequently, zero.



(a) (b)

Fig. 7: Device performance for different t_p: (a) I_{ON}/I_{OFF} ratio and *SS*, (b) V_t and f_{Tmax}.

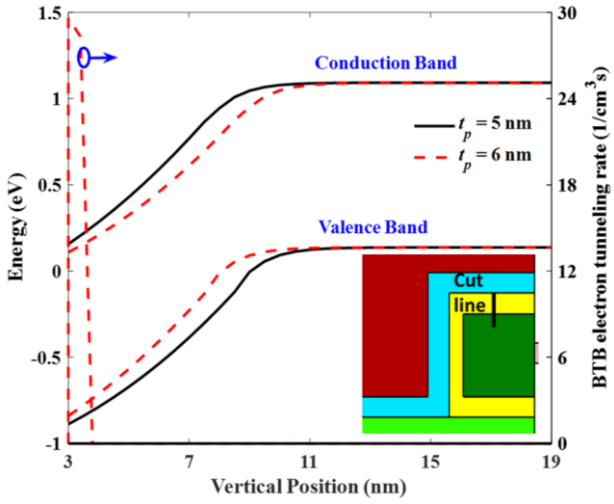
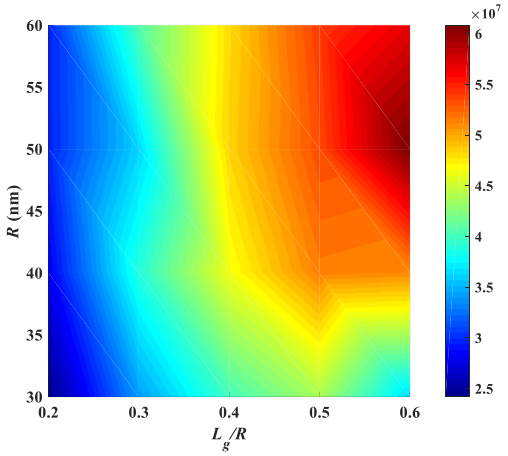


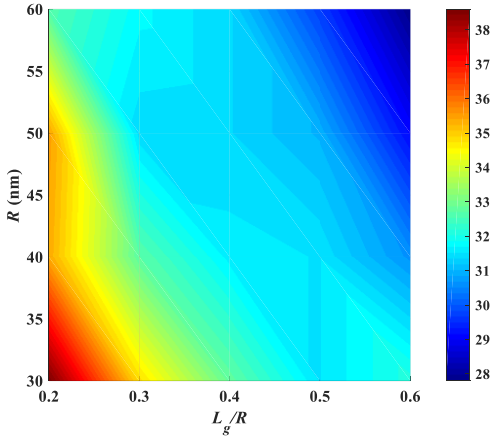
Fig. 8: Energy band diagrams from pocket to source region (at a horizontal distance of *R*/2) at OFF state (V_{DS} = 1 V and V_{GS} = 0 V).

Impact of L_g and R

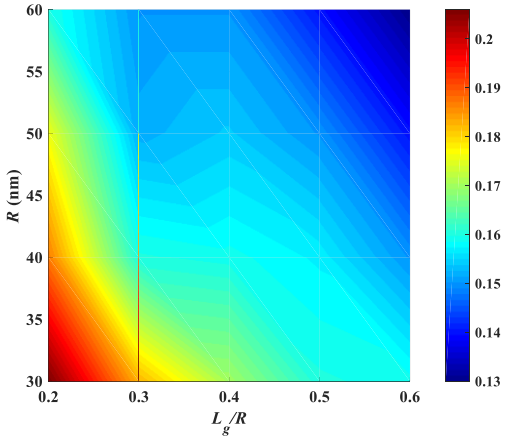
L_g and R are of significant influence on device performance which is clear from Fig. 9. Increasing the ratio L_g/R increases the ON/OFF current ratio (Fig. 9(a)) and f_{Tmax} (Fig. 9(d)) while it decreases both V_t (Fig. 9(b)) and SS (Fig. 9(c)). So, it is favorable to increase the ratio L_g/R. The optimum choice for L_g is equal to 60% of the radius. Regarding the variation of R, the ON/OFF current ratio increases as R increases up to R = 50 nm and then slightly decreases. Further, the higher R is favorable for both V_t and SS while it is undesirable for f_{Tmax}. So, a compromise should be met in order to choose the most suitable value for R. A suitable value of R = 50 nm could be chosen which gives the maximum ON/OFF current ratio and reasonable values for the other performance parameters.

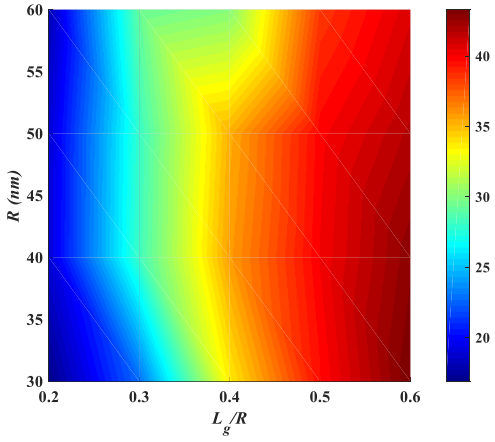


(a)



(b)





(c) (d)

Fig. 9: Device performance for different R and L_g/R ratios (a) I_{ON}/I_{OFF}, (b) SS (mV/decade), (c) V_t (V) and (d) f_{Tmax} (GHz).

Conclusion

In this work, through using Silvaco TCAD simulations, the SAA-TFET is proposed and designed comprehensively. We demonstrated that the ON current is high compared with conventional TFET due to tunneling in both vertical and horizontal directions. The study included varying different device parameters such as R, L_g, H_s, H_{ch} and t_p. Effects of these factors on the performance parameters such as the ON and OFF currents, I_{ON}/I_{OFF} ratio and SS are listed and analyzed. In addition, the cutoff frequency, as a FOM for analog performance, has been studied. The pocket width provides optimum performance at 5 nm. Further, it was found that the device performance is highly dependent on the ratio of L_g to R. The results show that the optimum performance is when L_g is 60% of the radius. The results reveal that the proposed structure provided high current, high f_T and lower SS. As a conclusion, it is expected that SAA-TFET can be one of the auspicious replacements for the next generation of tunneling devices in low-power and analog applications.

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